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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/813,501	03/31/2004	Alan R. Ball	ONS00555	4897

7590 07/29/2005

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EXAMINER	
TRA, ANH QUAN	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 07/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/813,501	BALL ET AL.	
	Examiner	Art Unit	
	Quan Tra	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/2/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-8 and 10-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Tsuchida. (US 2003/0197532).

As to claim 1, Tsuchida discloses in figure 6 a method of forming a self-gated transistor comprising: coupling a transistor (4, 5) operable to form a sense signal representative of a current through the self-gated transistor; and coupling a comparator (9) to receive the sense signal and responsively control the self-gated transistor based upon a polarity of the sense signal.

As to claim 2, figure 6 shows that forming the transistor operable to form the sense signal representative of the current through the self-gated transistor includes forming a transistor having a main transistor portion (4) and a sense transistor (5) as a sensing portion including coupling the main transistor portion to the sensing portion wherein the sensing portion is operable to form the sense signal representative of the current through the self-gated transistor.

As to claim 3, figure 6 shows that the step of coupling the main transistor portion to the sensing portion includes coupling a drain of the sense transistor to a drain of the main transistor portion and to the drain of the self-gated transistor and also including coupling a gate of the sense transistor to a gate of the main transistor portion and to the gate of the self-gated transistor.

As to claim 4, figure 6 shows that the step of coupling the comparator to receive the sense signal includes coupling an inverting input of the comparator to receive the sense signal (at node between 5 and 6).

As to claim 5, figure 6 shows that the step of coupling the comparator to receive the sense signal includes coupling a non-inverting input of the comparator to have a negative offset voltage.

As to claim 6, figure 6 shows that the step of coupling the comparator to receive the sense signal and responsively drive the self-gated transistor based upon a polarity of the sense signal includes coupling the comparator to responsively enable the self-gated transistor when the sense signal forms a voltage that is less than a voltage of a source of the self-gated transistor.

As to claim 7, figure 6 shows that the step of coupling the comparator to receive the sense signal includes coupling one of a diode or a resistor (6) between a source of a sense transistor and a source of the self-gated transistor.

As to claim 8, figure 6 shows a method of operating a self-gated transistor comprising: providing an MOS transistor having a main transistor portion (4) and a sensing portion (5) including coupling the main transistor portion to the sensing portion wherein the sensing portion is operable to form a first sense signal representative of a first current through the main transistor portion; detecting (by 9) the first sense signal and responsively disabling the self-gated transistor; conducting a second current through the sensing portion as a second sense signal wherein the second current flows in a direction opposite to the first current; and detecting the second sense signal and responsively enabling the self-gated transistor (the direct of the current the flows

through resistor 6 when transistor 5 is off is opposite with the direct of current the flows through resistor 6 when transistor 5 is on).

As to claim 10, figure 6 shows that the step of conducting the second current through the sensing portion as the second sense signal includes conducting the second sense current to flow through a resistor.

As to claim 11, figure 6 shows that the step of detecting the first sense signal and responsively disabling the self-gated transistor includes receiving the first sense signal on an input of a comparator (9).

As to claim 12, figure 6 shows a self-gated transistor comprising: a transistor having a main transistor portion (4) and a sensing portion (5) wherein the sensing portion is coupled to the main transistor portion to form a sense signal representative of a current through the self-gated transistor, the main transistor portion having a first gate; and a comparator (9) coupled to receive the sense signal and drive the first gate.

As to claim 13, figure 6 shows that the comparator has an inverting input coupled to receive the sense signal.

As to claim 14, figure 6 shows that the comparator has a non-inverting input coupled to a source of the self-gated transistor.

As to claim 15, figure 6 shows that the non-inverting input of the comparator has a negative offset voltage.

As to claim 16, figure 6 shows that the sensing portion is a portion of the main transistor portion with a source of the sensing portion separated from a source of the main transistor portion and wherein the main transistor portion and the sensing portion have a common drain.

As to claim 17, figure 6 shows the sensing portion having a source that is separate from a source of the main transistor portion and a protection circuit (6) coupled to the source of the sensing portion.

As to claim 18, figure 6 shows that a source of the main transistor portion is coupled to a source of the self-gated transistor.

As to claim 19, figure 6 shows a voltage regulator coupled to provide an operating voltage to the comparator and coupled to a source of the self-gated transistor (it is inherent that there is a circuit the provides supply voltage to the comparator).

As to claim 20, figure 6 shows that the self-gated transistor formed in a package having no greater than four leads.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tsuchida. (US 2003/0197532) in view of Fujihira (USP 5422593).

Tsuchida's figure 6 shows all limitations of the claim except for the step of conducting the second current through the sensing portion as the second sense signal includes conducting the second current to flow through a diode. However, Fujihira's figure 9 shows a method of using diode (31) for replacing resistor 31 in figure 4 as sense resistance. Therefore, it would have been

obvious to one having ordinary skill in the art to replace Tsuchida's resistor 6 with diode for the purpose of further protecting the sense resistor 5.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. These references are cited as interest because they show some circuits analogous to the claimed invention.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 571-272-1755. The examiner can normally be reached on 8:00 A.M.-5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

QUAN TRA
PRIMARY EXAMINER
ART UNIT 2816

July 28, 2005